

Fig. 1

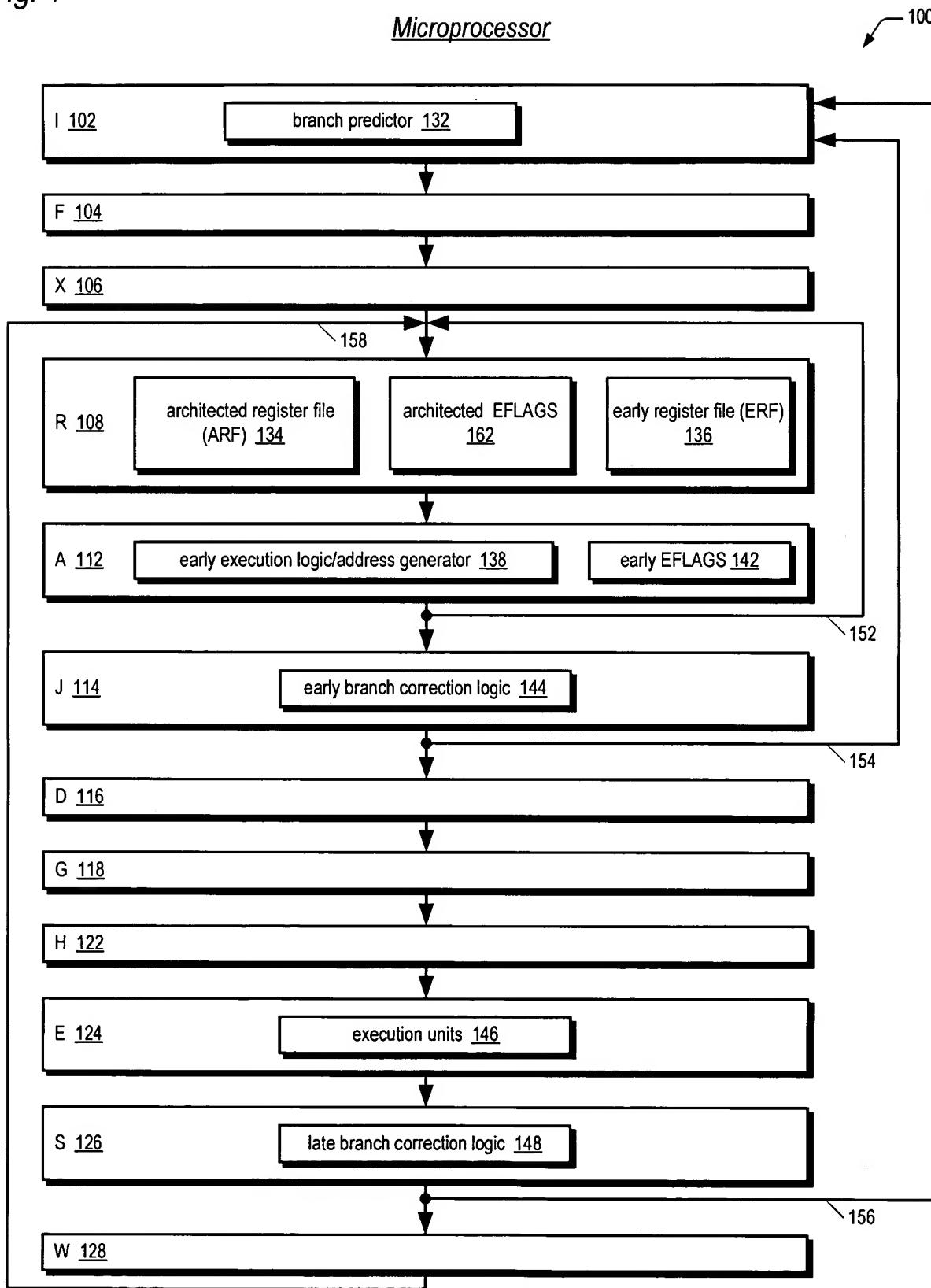
Microprocessor

Fig. 2

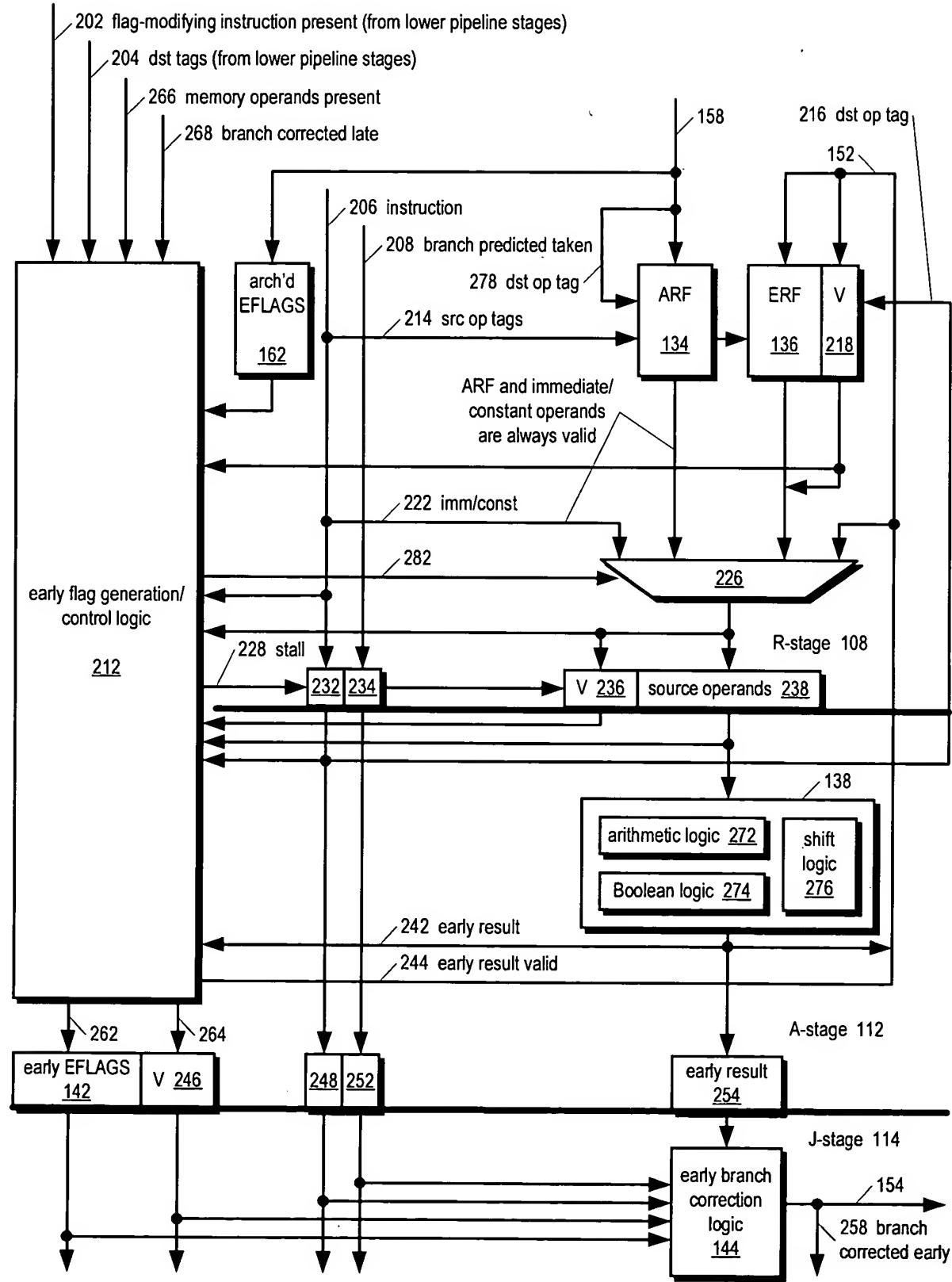
Microprocessor

Fig. 3

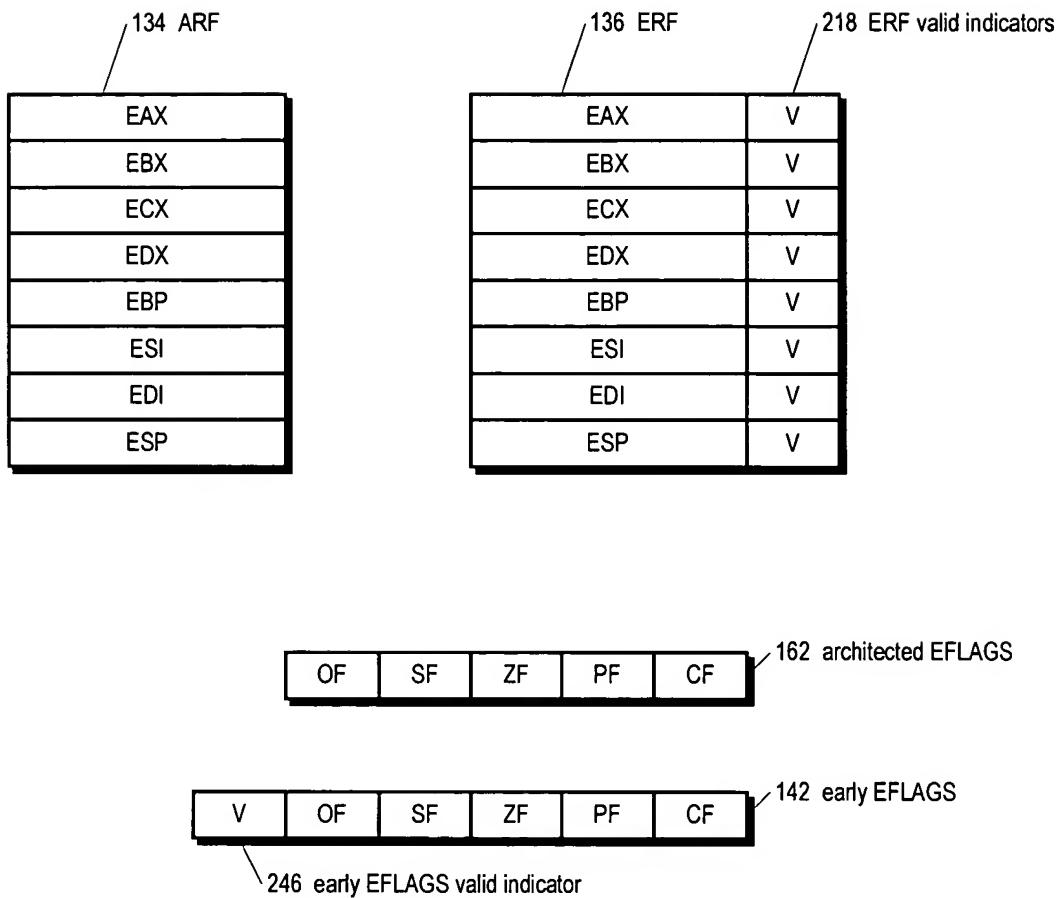
Architected Register File, Early Register File,Architected EFLAGS, Early EFLAGS

Fig. 4A

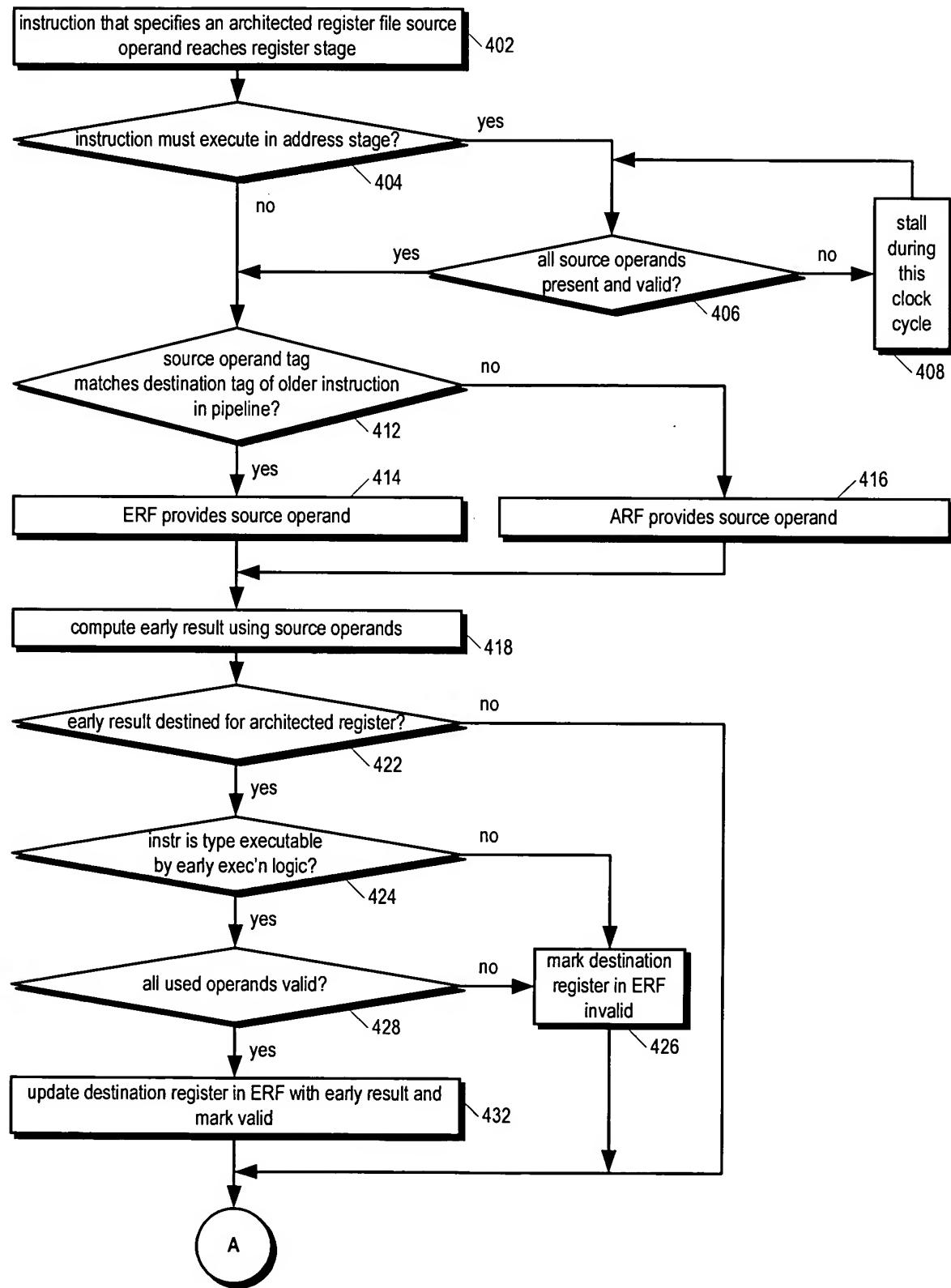
Early Result and Flag Operation

Fig. 4B

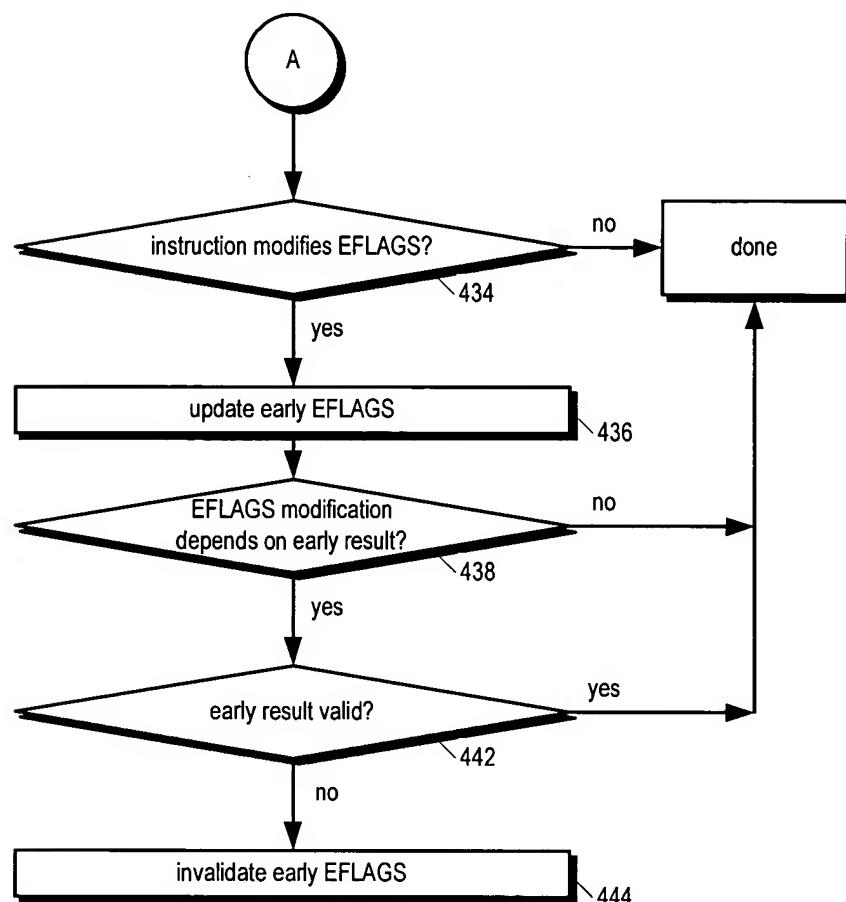
Early Result and Flag Operation (cont'd)

Fig. 5

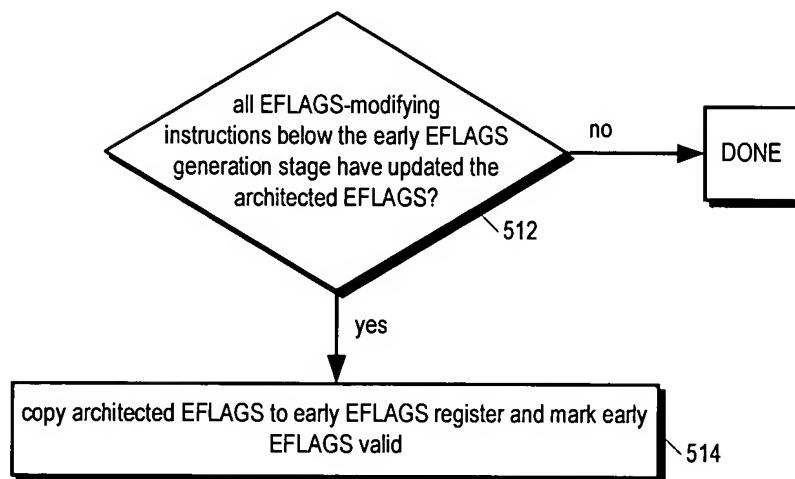
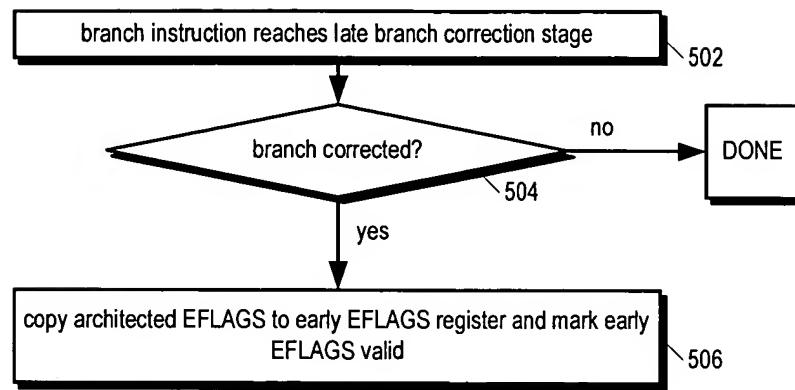
Early Flag Restore Operation

Fig. 6

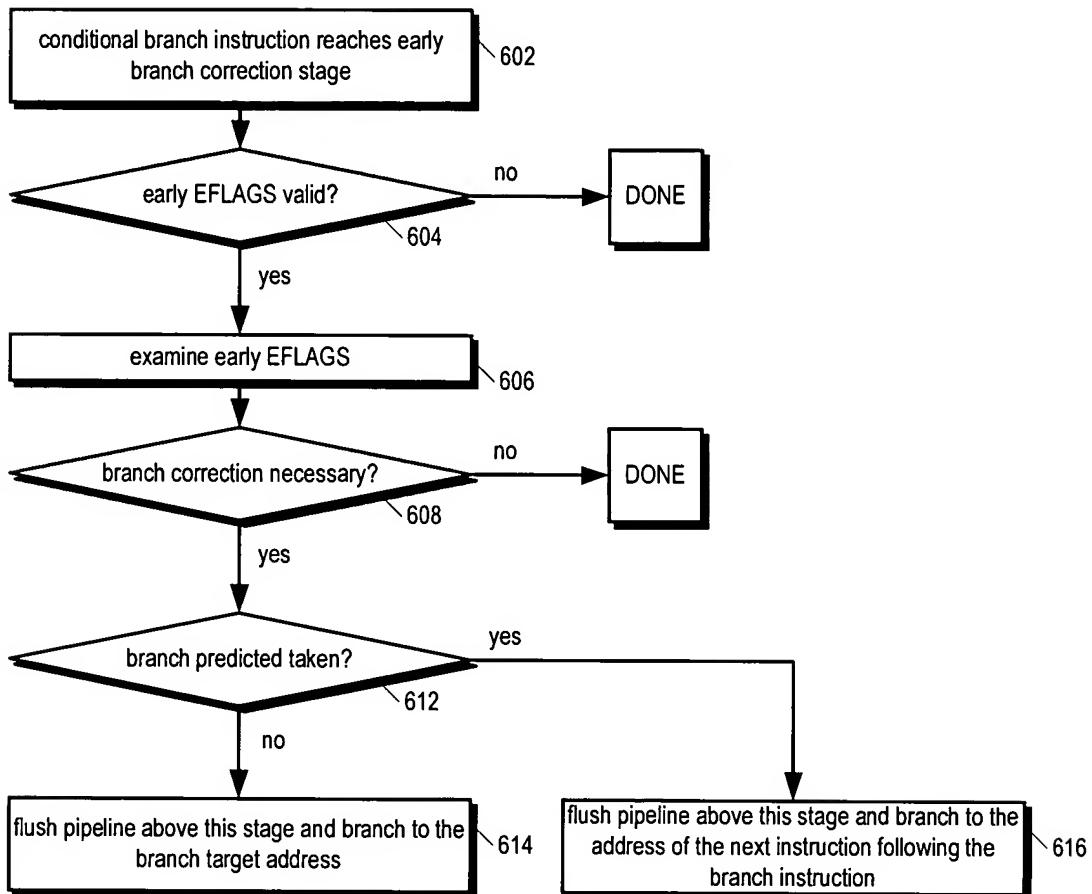
Early Branch Correction

Fig. 7

Late Branch Correction